

Hot Spot Detection in Integrated Circuits Laterally Accessing to their Substrate Using a Laser Beam

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Abstract- This work presents an approach to detect hot spots in active Integrated Circuits (IC) and devices. It is based on sensing the hot spot heat-flux within the chip substrate with a probe-laser beam. As the beam passes through the die, it experiences a deflection directly proportional to the heat-flux found along its trajectory (Internal InfraRed-Laser Deflection technique, IIR-LD). The proposed strategy allows inspecting the chip through its lateral sides (lateral access), avoiding the metal and passivation layers placed over the die.

I. INTRODUCTION

The scaling down of CMOS technologies has enabled a whole system to be integrated on a single Silicon chip (System on a Chip, SoC). A drawback of these high integration levels is the loss of observability that it entails, since only few nodes are electrically accessible from outside. Sensing temperature for localising hot spots provides additional observability in nowadays integrated circuits (ICs) in several scenarios. On the one hand, hot spots have been classically related with IC failure analysis [1]. On the other hand, the location of unexpected hot spots may be used to increase analog [2] or digital [3] system performance in system debugging. Moreover, the exact location of hot spots can be used as an indicator of the fabrication process dispersion in nanometric technologies [4].

Mostly, two off-chip monitoring approaches have been extensively used in ICs: Chip surface thermometries (e.g., Infrared thermography) [5] and MOSFET hot-carriers' luminescence detection [6]. Both measure the temperature field and luminescence emission from the chip topside (frontside measurements). However, these magnitudes may be strongly or totally attenuated by metal or passivation layers in current IC technologies [5, 6]. Several techniques have been proposed to overcome these challenges, e.g.: interferometric measurements [7] or backside thermal imaging [8]. The situation is more restrictive when a packaged IC is intended to be studied: There is no access through the chip's frontside or backside to monitor hot spots by off-chip techniques.

This paper is addressed to the location of hot spots by sensing the thermal gradients that are induced into the IC substrate. The thermal gradients can be measured by inspecting the IC through its lateral side (perimeter scanning) with an InfraRed (IR) laser probe ($\lambda = 1310\text{nm}$),

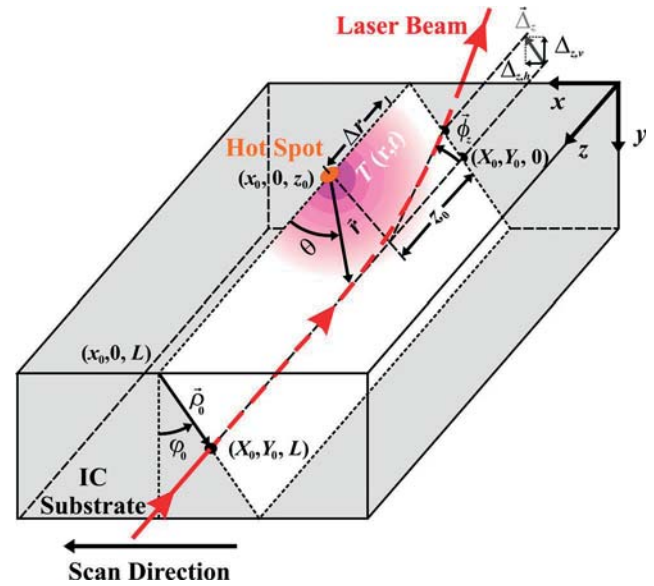


Fig. 1. IC with a hot spot whose perimeter is scanned with a laser beam probe. All the related geometrical variables and magnitudes are also presented.

avoiding the metal and passivation layers placed over the Silicon [9, 10]. When the laser beam traverses the substrate of an IC under test (CUT) at a given depth (inspection depth), it experiences a deflection proportional to the thermal gradient found along its trajectory, since it induces a refractive index gradient (Mirage effect). The proposed strategy allows inspecting the chip through its lateral sides (lateral access), avoiding the metal and passivation layers placed over the die. The obtained results demonstrate the suitability of this technique to locate and characterise devices behaving as hot spots in nowadays IC CMOS technologies.

II. TECHNIQUE'S PHYSICAL PRINCIPLE

Fig. 1 illustrates the trajectory angular deflection ϕ_z experienced by the laser probe due to the Mirage effect when a die is laterally inspected through its substrate along the lateral coordinate x at a given inspection depth Y_0 . This figure also shows a heat source located at $(x_0, 0, z_0)$ that generates a thermal field $T(r,t)$ responsible of the beam deflection.

When the hot spot dissipates a power that can be expressed as a sinusoidal waveform, it is possible to consider the silicon substrate as a semi-infinite medium by selecting the suitable working frequency value f (see Fig. 1). In this situation, when the heat source dimensions are small compared to the silicon substrate ones (punctual heat source approximation), the temperature distribution can be assumed radial with spherical symmetry. As a result of that, the laser beam trajectory within the die is always contained in the plane defined by the heat source location and the laser beam insertion point [11] (see Fig. 1). Once the laser probe has traversed the IC substrate, its trajectory has experienced a total deflection $\bar{\Delta}_z$. $\bar{\Delta}_z$ can be decomposed into its x - and y -Cartesian components (see Fig. 1), referred as horizontal and vertical ($\Delta_{z,h}$ and $\Delta_{z,v}$, respectively). By monitoring $\Delta_{z,h}$ and $\Delta_{z,v}$ with a deflection sensing system, the hot spots are located accurately.

The temperature gradient generated inside the silicon substrate $\nabla T(r,t)$ is as well an harmonic function and obeys the following equation outside of the power generation region [12]:

$$\nabla T(r,t) = \text{Re}[-C_f(1+r\xi)/r^2 \exp(-r\xi + i2\pi kft)] \hat{u}_r \quad (1)$$

where C_f refers to a constant associated to the frequency f , r corresponds to the distance from the heat source, and \hat{u}_r represents the unit vector corresponding to the radial direction from the heat source (see Fig. 1). ξ is a complex constant which depends on f and the material thermal diffusivity D_α as:

$$\xi = (1+i)\sqrt{\pi kf/D_\alpha} \quad (2)$$

From Eqs. (1) and (2), it can be seen that $\nabla T(r,t)$ is frequency and position dependent, e.g., its amplitude decreases as f and r increases. To determine the penetration depth of the thermal energy into the IC substrate, a characteristic depth d_p is defined as $d_p = \sqrt{D_\alpha/(\pi kf)}$, which corresponds to the thermal diffusion length [12]. Consequently, $T(r,t)$ and $\nabla T(r,t)$ are confined within the substrate in a hemisphere of radius Δr , which can be expressed as a multiple of d_p , i.e., $\Delta r = m d_p$ (see Fig. 1) [12, 13]. Thus, by selecting a suitable value for the product kf , the radius of the thermal disturbance can be externally controlled with high accuracy.

The thermal gradient $\nabla T(r,t)$ inside the IC substrate induces a refractive index gradient ($\nabla n(r,t)$) as follows (thermo-optical effect [14]):

$$\nabla n(r,t) = \frac{\partial n}{\partial T} \nabla T(r,t) \quad (3)$$

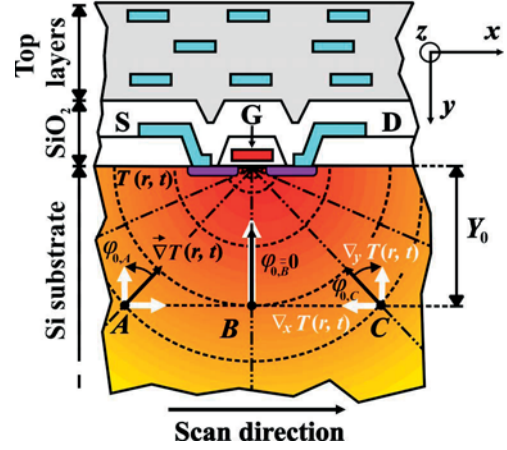


Fig. 2. Temperature field ($T(r,t)$, black dashed lines) and its thermal gradient vectors ($\nabla T(r,t)$, black solid vectors) in the IC substrate caused by a MOSFET acting as a punctual heat source. Horizontal and vertical Cartesian components of $\nabla T(r,t)$ ($\nabla_x T(r,t)$ and $\nabla_y T(r,t)$, white solid vectors) are also depicted. The scan is performed along the x coordinate at a given depth Y_0 for several inspecting points (A, B, and C).

where $\partial n/\partial T$ is the thermo-optical coefficient ($2.0 \times 10^{-4} \text{ K}^{-1}$ in Silicon [14]). As a consequence, $\nabla n(r,t)$ provokes the deflection of the laser beam towards the heat source location [11].

According to these dependencies, let's consider the temperature gradient vectors represented in Fig. 2 at the points labelled A, B and C, placed at a depth Y_0 within the substrate of an IC with a small transistor dissipating power. This figure displays $\nabla T(r,t)$, jointly with its horizontal and vertical components ($\nabla_x T(r,t)$ and $\nabla_y T(r,t)$, respectively). The points A, B, and C are positioned respect to the heat source by using φ_0 (i.e., see $\varphi_{0,A}$, $\varphi_{0,B}$, $\varphi_{0,C}$ in Fig. 2). $\nabla_x T(r,t)$ and $\nabla_y T(r,t)$ are related to the module of $\nabla T(r,t)$ ($\|\nabla T(r,t)\|$), as follows:

$$\nabla_y T(r,t) = -\|\nabla T(r,t)\| \cdot \cos(\varphi_0) \quad (4)$$

$$\nabla_x T(r,t) = \|\nabla T(r,t)\| \cdot \sin(\varphi_0) \quad (5)$$

where $\varphi_0 = \tan^{-1}((X_0 - x_0)/Y_0)$. Focusing on $\nabla_y T(r,t)$, it is clear that its maximum amplitude is at the point B (i.e., $\varphi_{0,B}=0$), placed beneath the hot spot. By contrast, the amplitude of $\nabla_x T(r,t)$ nulls at B. Therefore, this extrema's behaviour of $\nabla_y T(r,t)$ and $\nabla_x T(r,t)$ will be detected by monitoring $\Delta_{z,h}$ and $\Delta_{z,v}$ with the experimental set-up described in the next section. This behaviour allows us to accurately locate the coordinates of the device acting as a hot spot along the axis defined by the scan direction.

In the case of performing the lateral scanning along the z -direction (laser propagates through x -direction), the definition of φ_0 should be modified changing $X_0 - x_0$ by $Z_0 - z_0$.

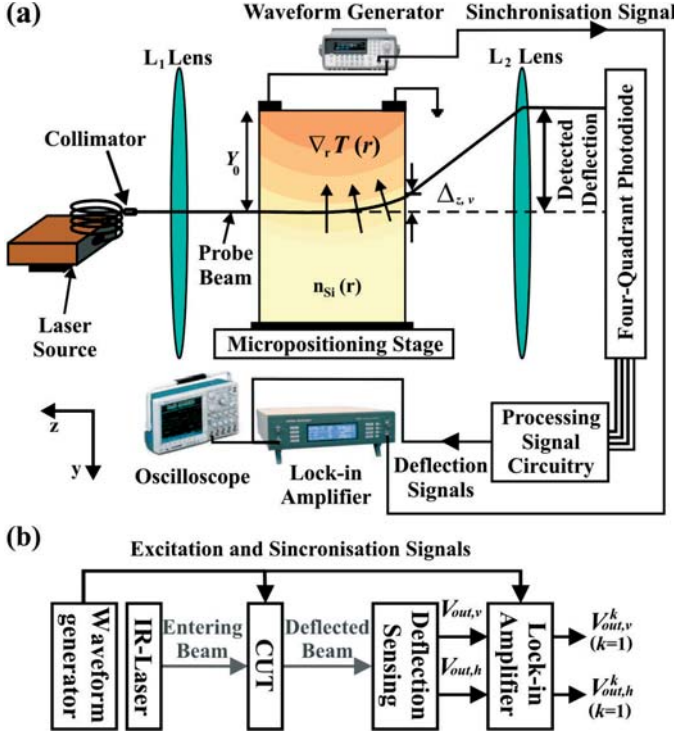


Fig 3. (a) Experimental rig schematic, reproducing the thermal and optical phenomena inside the IC during measurements. (b) Block diagram schematising the derivation of the harmonic components of the beam deflection signals.

III. EXPERIMENTAL APPROACH

Figs. 3 (a) and (b) schematically depict the experimental rig and the signals originated from a beam deflection measurement, respectively. The experimental rig is composed by three elementary functional set-ups, called optical, electrical, and mechanical (see Fig. 3 (a)). The optical set-up comprises an IR-laser source (1310 nm), two converging lenses (L_1 and L_2), and a beam collimator. The electrical set-up includes the CUT excitation system (33120A Agilent function waveform generator), the deflection sensing system, and the acquiring signal equipment (SR 7265 DSP lock-in amplifier and TDS5034B Tektronix oscilloscope). The deflection sensing system [15] consists of a Germanium four-quadrant photodiode sensor (J16QUAD-8D6-R05M, Judson Technologies), an I/V converter (FQP preamplifier), and a post-processing signal circuit (see Fig. 3 (a)). The mechanical set-up is constituted by micro-positioning stages, adapting mechanical pieces, and an optical breadboard. For more details, this experimental rig and the measurement procedure are reported in Refs. 9, 10, and 16.

Fig. 3 (b) summarises the measurement sequence and all the involved signals. This figure schematically depicts how the beam probe enters to the CUT substrate, it deflects and its deviation is eventually detected by the deflection sensing system. As a result, two electrical signals proportional to $\Delta_{z,h}$ and $\Delta_{z,v}$ ($V_{out,v}$ and $V_{out,h}$, respectively) are directly obtained [15, 16]. If the dissipating device is activated with a periodic signal, the vertical and horizontal deflection signals can be expressed in a Fourier series, where each harmonic is

labelled with the superscript k (see Fig. 3 b). With the lock-in amplifier, the amplitude of the first harmonic ($k=1$) is selectively determined, which show the following proportionality relationship with $\|\nabla T(r,t)\|$ and the angular coordinate φ_0 :

$$|V_{out,v}^1| \propto \|\nabla T(r,t)\| \cos(\varphi_0) \quad (6)$$

$$|V_{out,h}^1| \propto \|\nabla T(r,t)\| \sin(\varphi_0) \quad (7)$$

In order to demonstrate the technique's feasibility, a specific integrated circuit ($3075 \times 2350 \times 500 \mu\text{m}^3$) has been developed and used to measure the thermal coupling generated by MOS transistors acting as hot spots (partially shown in Figs. 4 (a) and (d)). In this IC, there are 16 dissipating devices consisting in MOS transistors (channel size $20 \times 1.2 \mu\text{m}^2$) connected in diode configuration, i.e., source tied to ground and gate connected to the drain. In addition, each gate is directly accessible through a pin, allowing individual activation. Each device can dissipate up to 28 mW. Fig. 4 (a) is a photograph of the analysed region of the IC showing 8 MOS transistors that may behave as hot spots. The square indicates the location of the specific MOS transistor used to generate the hot spot. The CUT preparation process has comprised two steps: Polishing its lateral walls and soldering it on a PCB board. Thereby, the IR-radiation transmission through the IC substrate is enhanced, while an easily biasing and handling of the CUT is ensured.

IV. EXPERIMENTAL RESULTS

In the experiments, the CUT has been stimulated in such a way that the power dissipated was periodic (5V voltage square waveform); with a frequency of 2120 Hz ($d_p=116 \mu\text{m}$ for $k=1$), and 25 mW of amplitude. All measurements have been performed at the inspection depth $Y_0=180 \mu\text{m}$, which is deeper than d_p ($116 \mu\text{m}$). In this way, an idea of the sensitivity level of this approach will be provided, since these measurement conditions are not the optimal ones. Namely, $\nabla T(r,t)$ is strongly attenuated at the selected Y_0 , expecting to detect low signal levels for $|V_{out,v}^1|$ and $|V_{out,h}^1|$.

Figs. 4 (b) and 4 (c) plot the normalised amplitudes of $V_{out,v}^1$ and $V_{out,h}^1$ after a perimeter scan along the directions x and z (see x and z coordinate definition in Fig. 1). When the IC perimeter is inspected (two lateral sides along the x and z axis), the device acting as a hot spot is located at the point where $|V_{out,v}^1|$ is maximum and $|V_{out,h}^1|$ nulls (see Figs. 4 (b) and 4 (c)). Notice that for determining the location of the hot spot, both conditions must be fulfilled. As a matter of fact, measuring only the vertical beam deflection signal should provide enough information to approximately detect the heat source. Nevertheless, measuring the horizontal beam deflection is mandatory to achieve micronic and submicronic spatial resolution. Due to both the chosen Y_0 and f values and the heat spreading effect (thermal diffusion mechanism), the summit of $V_{out,v}$ is not sharp enough to achieve the desired

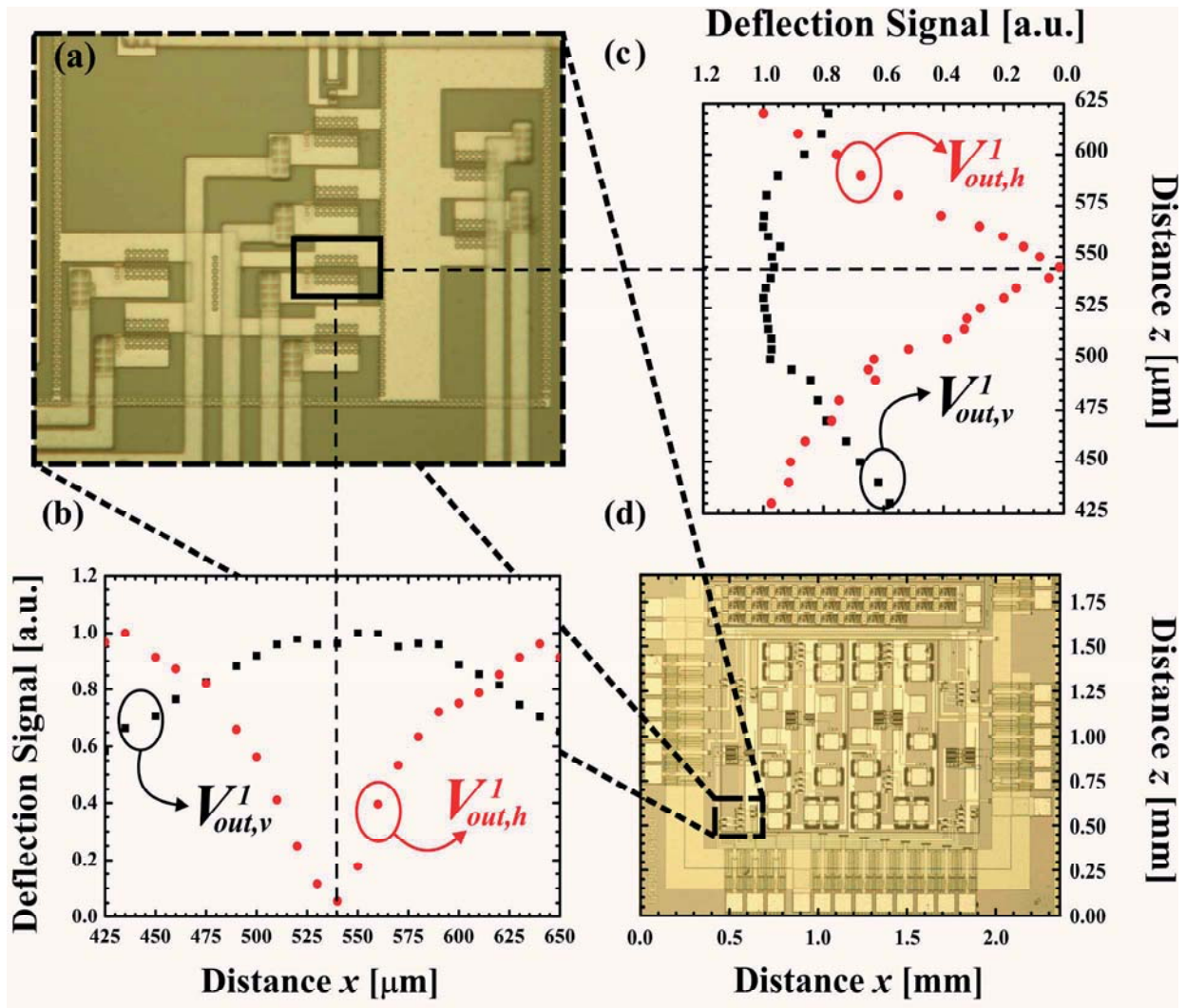


Fig 4. (a) Photograph of the region of the chip layout where a MOS transistor behaves as a hot spot. (b) Amplitude of the vertical and horizontal beam deflection components for $k=1$ as a function of the IC layout x coordinate. (c) Amplitude of the vertical and horizontal beam deflection components for $k=1$ as a function of the IC layout z coordinate. The maximum in the vertical component and the minimum in the horizontal component in both scan directions locate the dissipating MOS transistor. (d) IC top view photograph, partially illustrating the IC dimensions and the coordinate system adopted in this work.

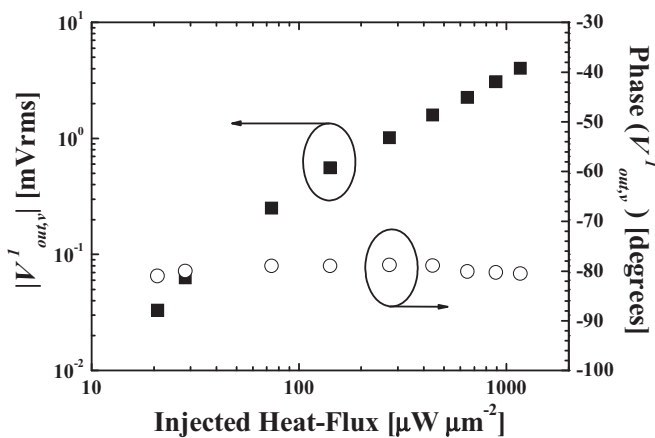


Fig 5. Dependence of the deflection signal (magnitude and phase) on the heat-flux dissipated by a MOSFET (0.5-28 mW power dissipation range), when measured exactly below the device at $Y_0=180 \mu\text{m}$.

resolution. In addition, should we consider experimental error sources such as, the local irregularities of the die lateral sides that modify laser transmissivity and the positioning error in the micropositioning system. The influence of all these effects on $V_{out,v}$ are observed in Figs. 4 (b) and 4 (c): Nearby the lateral position of the device acting as a hot spot, some fluctuations are visible. However, in the surroundings corresponding to the maximum in $|V_{out,v}^1|$, it is observed that

$|V_{out,h}^1|$ nullifies, univocally indicating the coordinates of the device acting as a hot spot. From the reported results, it is worth to point out that far beyond d_p , it is also possible to determine thermal information. Therefore, the limitation at the selected inspection depth is the threshold imposed by the minimum signal to noise ratio detectable with the deflection sensing system.

In order to experimentally determine which are the lower detection limits in the experimental conditions defined



6-8 October 2010, Barcelona, Spain

above, further measurements at $Y_0=180\text{ }\mu\text{m}$ have been conducted beneath the dissipating transistor (therefore, $V_{out,h}^1=0$). Fig. 5 plots the measured $V_{out,v}^1$ (amplitude and phase), as a function of the heat flux injected into the IC substrate. Heat flux is considered because this magnitude is proportional to the thermal gradient (Fourier's law). Fig. 5 reports the results that the minimum detectable voltage with the lock-in amplifier is $33\text{ }\mu\text{Vrms}$, which corresponds to $0.84\text{ }\mu\text{W }\mu\text{m}^{-2}$ heat-flux amplitude at the inspection depth. This happens when the device dissipates 0.5 mW ($21\text{ }\mu\text{W }\mu\text{m}^{-2}$ on the top). Moreover, it is interesting to notice that the slope of the sensed signal and the injected heat-flux on the top is the unity, which agrees with theory. On the other hand, the phase of the sensed flux is constant and independent of the amplitude of the injected flux, which justifies that thermal information is measured.

V. CONCLUSION

This work shows an alternative approach to locate hot spots in ICs. It consists in sensing the thermal gradient generated by the hot spot laterally accessing to the die with a laser beam. Due to the thermo-optical effect, the laser beam is deflected (Mirage effect). The beam deviation is proportional to the thermal gradient found along the laser propagation direction within the IC substrate. We have experimentally demonstrated that the horizontal component of the beam deflection provides a higher spatial resolution than the vertical one when measurements are performed beyond the thermal flux diffusion length (worst case scenario). Besides, experimental results show how a heat source is located at inspection depths higher than two orders of magnitude ($Y_0=180\text{ }\mu\text{m}$) of its lateral dimensions ($1.2\text{ }\mu\text{m}$). This strategy is a good solution when temperature is strongly attenuated by metal or passivation layers or there is no access by the chip's frontside or backside to monitor hot spots when employing off-chip techniques. Additionally, the die lateral access allows inspecting big ICs more rapidly than other methods, as only the perimeter of the die is scanned. Measuring simultaneously the vertical and horizontal beam deflection improves accuracy and speed in the process of locating devices, structural faults, IC functional units, or interconnects acting as hot spots. This technique is applicable to any IC without the need to have an electrical node to excite the hot spot, since it can be externally stimulated by introducing a modulation signal through the same IC power supply pad, for instance.

As another potential application, this technique not only allows thermally evaluating any complex IC (e.g., a system on chip), in which there are different temperature's frequency components coming from several circuitries monolithically integrated, but also could permit characterising its electromagnetic interactions. This application could be an interesting option to study electromagnetic coupling in ICs by means of temperature measurements through the substrate. This technique is also promising for the thermal analysis of RF devices showing narrow gate fingers (such as Silicon-based LDMOS, SiC-

based MESFETs or AlGaIn/GaN-based HEMTs), in which high-resolution thermography is difficult to implement.

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REFERENCES

- [1] M. Pedram and S. Nazarian, "Thermal modeling, analysis, and management in VLSI circuits: Principles and methods", *P. IEEE*, vol. 94, n° 8, pp. 1487-1500, Aug. 2006.
- [2] S. Mattisson, H. Hagberg, and P. Andreani, "Sensitivity Degradation in a Tri-Band GSM BiCMOS Direct-Conversion Receiver", *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 486-496, Feb. 2008.
- [3] S.A. Bota, J.L. Rossello, C. de Benito, A. Keshavarzi, and J. Segura, "Impact of Thermal Gradients on Clock Skew and Testing", *IEEE Des. Test Comp.*, vol. 23, no. 5, pp. 414-424, May 2006.
- [4] J. Jaffari and M. Anis, "Statistical Thermal Profile Considering Process Variations: Analysis and Applications", *IEEE T. Comput. Aid. D.*, vol. 27, no. 6, pp. 1027-1040, June 2008.
- [5] J. Altet, W. Claeys, S. Dilhaire, and A. Rubio, "Dynamic surface temperature measurements in ICs", *P. IEEE*, vol. 94, no. 8, pp. 1519-1533, Aug. 2006.
- [6] S. Bianic, S. Allemand, G. Kerros, P. Scafidì, and D. Renard, "Advanced backside failure analysis in 65 nm CMOS technology", *Microelectron. Reliab.*, vol. 47, no. 9-11, pp. 1550-1554, Sept.-Nov. 2007.
- [7] J. Altet, M. A. Salhi, S. Dilhaire, A. Syal, and A. Ivanov, "Localisation of devices acting as heat source in ICs covered entirely by metal layers", *Electron. Lett.*, vol. 39, no. 20, pp. 1440-1441, Oct. 2003.
- [8] G. Tessier, M. Bardoux, C. Boué, C. Filloy, and D. Fournier, "Back side thermal imaging of integrated circuits at high spatial resolution", *Appl. Phys. Lett.*, vol. 90, no. 17, pp. 171112 (3 pages), Apr. 2007.
- [9] X. Perpiñà, X. Jordà, N. Mestres, M. Vellvehi, P. Godignon, J. Millán, and H. von Kiedrowski, "Internal infrared laser deflection system: a tool for power devices characterization", *Meas. Sci. Technol.*, vol. 15, no. 5, pp. 1011-1018, Oct. 2004.
- [10] X. Perpiñà, X. Jordà, F. Madrid, M. Vellvehi, J. Millán, and N. Mestres, "Transmission Fabry-Perot interference thermometry for thermal characterisation of microelectronic devices", *Semicond. Sci. Tech.*, vol. 21, no. 12, pp. 1537-1542, Dec. 2006.
- [11] M. Born and E. Wolf, *Principles of Optics*, Exeter, Pergamon Press (6th edition), 1989.
- [12] H. S. Carslaw, and J. C. Jaeger, *Conduction of Heat in Solids*, Oxford, Clarendon Press (2nd edition), 1986.
- [13] J. Altet, J. M. Rampnoux, J. C. Batsale, S. Dilhaire, A. Rubio, W. Claeys, and S. Grauby, "Applications of temperature phase measurements to IC testing", *Microelectron. Reliab.* vol. 44, no. 1, pp. 95-103, Jan. 2004.
- [14] A. N. Magunov, "Temperature dependence of the refractive index of silicon single crystal in the 300-700 K range", *Opt. Spectros.*, vol. 73, no. 2, pp. 205-206, Aug. 1992.
- [15] X. Perpiñà, X. Jordà, M. Vellvehi, J. Millán and N. Mestres, "Development of an analogue processing circuit for ir-radiation power and non-contact position measurements", *Rev. Sci. Instrum.*, vol. 76, no. 2, 025106 (6 pages), Feb. 2004.
- [16] X. Perpiñà, *Power Devices Electrothermal Characterisation by Optical Techniques - An Experimental Approach to Analyse Internal Electrothermal Phenomena at Device Level*, Saarbrücken, VDM Verlag Dr. Mueller e.K., April 2008.